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ABSTRACT OF THE DISCLOSURE

A multi-bank testing apparatus for a synchronous DRAM, which allows all banks of the synchronous DRAM to simultaneously carry out their write and read operations in a test mode, thereby being capable of testing the entire bank in order to reduce the test time being likely to increase in accordance with an increased memory integration degree. The multi-bank testing apparatus includes a row address strobe generating unit for enabling a word line to transmit data from cells to bit line sense amplifiers in each bank of the synchronous DRAM, a column address strobe generating unit for generating a signal adapted to enable transistors respectively adapted to couple bit lines carrying data, amplified by the bit line sense amplifiers, to local data bus lines, input/output sense amplifiers for amplifying data on the local data bus lines, respectively, a transmission gate unit for controlling transmission of data from the input/output sense amplifiers to global read data bus lines, and an input/output comparing unit for compressing data from the input/output sense amplifiers prior to the transmission thereof to the global read data bus lines.